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Sanders

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

T. MIYAMOTO et al

Serial No. 09/530,490 Group Art Unit: 2814

Filed: April 28, 2000 Examiner: D. Graybill

For: SEMICONDUCTOR DEVICE AND PROCESS FOR MANUFACTURING THE SAME

AMENDMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

In response to the Office Action dated July 5, 2001, please amend the above-identified application as follows. A two-month Extension of Time accompanies this response.

IN THE CLAIMS

Please cancel claims 1-19 and 30-33 without prejudice or disclaimer and add new claims 34-37 as follows.

34. (New) A chip scale package, provided by dividing a semiconductor wafer along scribe lines defining a plurality of chip scale package forming areas in said semiconductor wafer, comprising:

(a) a semiconductor chip having a main surface, a rear surface opposite to said main surface and a surface passivation film to cover said main surface, said

semiconductor chip having a plurality of semiconductor elements and bonding pads formed on said main surface thereof, said bonding pads being exposed from said surface passivation film;

(b) an elastomer layer formed on said surface passivation film to cover said main surface of said semiconductor chip and to expose said bonding pads, said elastomer layer having an elastic modulus relatively lower than said surface passivation film;

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(c) conductive layers formed on said elastomer layer, first ends of said conductive layers being disposed on said elastomer layer and second ends of said conductive layers being electrically connected to the corresponding ones of said bonding pads; and

(d) a plurality of bump electrodes formed on said elastomer layer, said plurality of bump electrodes being electrically connected to said first ends of said conductive layers.

35. (New) A chip scale package according to claim 34, wherein said bump electrodes are solder bump electrodes.

36. (New) A chip scale package according to claim 34, wherein said elastomer layer has an elastic modulus of about 1 to 500 Mpa.

B1 37. (New) A chip scale package according to claim 34, wherein said conductive layers are formed by plating.

REMARKS

Claims 1-19 and 30-33 have been canceled without prejudice or disclaimer. New claims 34-37 have been added. Accordingly, claims 34-37 are currently pending in the application.

Applicants appreciate the Examiner's acknowledgement of the claim for priority under 35 U.S.C. § 119.

The rejections of the claims under 35 U.S.C. §112, second paragraph and 35 U.S.C. §103 have been rendered moot the by cancellation of claims 1-19 and 30-33 in favor of new claims 34-37. It is submitted that these new claims satisfy 35 U.S.C. §112 and are patentable over the cited art.

New claim 34 recites a chip scale package, provided by dividing a semiconductor wafer along scribe lines defining a plurality of chip scale package forming areas in the semiconductor wafer. The chip scale package includes a semiconductor chip having a main surface, a rear surface opposite the main surface and a surface passivation film covering the main surface. The semiconductor chip has a

plurality of semiconductor elements and bonding pads formed on its main surface with the bonding pads being exposed from the surface passivation film. An elastomeric layer is formed on the surface passivation film to cover the main surface of the semiconductor chip and to expose the bonding pads. The elastomeric layer has an elastic modulus relatively lower than the surface passivation film. Conductive layers are formed on the elastomeric layer. First ends of the conductive layers is disposed on the elastomeric layer and the second ends of the conductive layers are electrically connected to the corresponding ones of the bonding pads. Finally, a plurality of bump electrodes are formed on the elastomeric layer and are electrically connected to first ends of the conductive layers.

By providing a chip scale package as set forth above, there is provided a resistance characteristic against thermal stress and at the same time realizing a compact size. None of the cited references disclose the above-mentioned features of the present invention.

For example, Wojnarowski et al disclose Wafer Level Integration having a plurality of chip areas 12 which are electrically connected to one another by conductors 21 so as to achieve one function of Wafer Level Integration. However, they do not disclose a chip scale package provided by dividing

a semiconductor wafer nor the presence of a row elastic modulus-elastomer layer having an elastic modulus relatively lower than the surface passivation film and being formed between the chip and the bump electrodes. In addition, groove 68 of Wojnarowski et al (see Figure 6) is formed so that the Wafer Layer Integration of a large area can be mounted on a concave portion. However, groove 68 does not divide wafer 10. Finally, Wojnarowski et al do not disclose that wafer 10 or chip areas 12 are mounted on the mounting substrate by any bump electrodes. Thus, Wojnarowski et al are not concerned with the concept of using a lower elastic-elastomer layer in reducing stress acting on the bump electrodes.

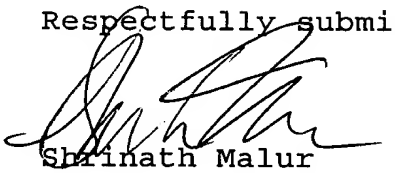
The deficiencies in Wojnarowski et al are not overcome by resort to the remaining references. Neither Iwasaki et al, Akagawa nor Lur et al disclose that the row elastic modulus-elastomer layer has an elastic modulus relatively lower than the surface passivation film and is formed between the chip and bump electrodes.

Therefore, any combination of these references, if possible, would not teach all of the limitations of the claimed invention. In addition, it is submitted that one of ordinary skill in the art would not be motivated to combine these references in the manner asserted because Wojnarowski et

al disclose Wafer Level Integration and substrate mounting without bump electrodes while references such as Iwasaki et al and Akagawa disclose a substrate mounting structure having bump electrodes.

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is in condition for allowance. Reconsideration and examination are respectfully requested.

Respectfully submitted,



Shrinath Malur
Registration No. 34,663
Attorney for Applicants

MATTINGLY, STANGER & MALUR
1800 Diagonal Rd., Suite 370
Alexandria, Virginia 22314
(703) 684-1120
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